APPENDIX
"Version with markings to show changes made."

Paragraph beginning page 4, line 5:

Figure 1 is a block diagram of a computer system incorporating the associative crossbar switch according to the preferred embodiment of this invention. The following briefly describes the overall preferred system environment within which the crossbar is incorporated. For additional information about the system, see [**copending U.S. Patent Application Serial No. _____, filed _____**] Application No. 08/422,753 filed April 13, 1995, which issued as U.S. Patent No. 5,560,028 on September 24, 1996; which is a continuation of Application No. 08/147,800 filed November 5, 1993, now abandoned, and entitled "Software Scheduled Superscaler Computer Architecture," which is incorporated by reference herein. FIG. 1 illustrates the organization of the integrated circuit chips by which the computing system is formed. As depicted, the system includes a first integrated circuit 10 that includes a central processing unit, a floating point unit, and an instruction cache.